

ATTORNEY DOCKET NO. 91-C-127C1 (STMI01-00022)  
U.S. SERIAL NO. 09/803,715  
PATENT

**REMARKS**

Claims 1 and 32-47 are pending in the present application.

Claims 46-47 are withdrawn from consideration.

Claims 1 and 38 were amended herein.

Reconsideration of the claims is respectfully requested.

Claims 1, 32, 35, 38-39 and 42 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,169,792 to *Kato et al.* Claims 33 and 40 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Kato et al* in view of U.S. Patent No. 4,110,899 to *Nagasawa et al.* Claims 34 and 41 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Kato et al* in view of *Nagasawa et al* and further in view of JP 63-271956 (*Hosaka*). Claims 36-37 and 43-45 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Kato et al* in view of *Nagasawa et al* and further in view of Wolf et al, *Silicon Processing For the VLSI Era, Vol. 2*. These rejections are respectfully traversed.

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. MPEP § 2142, p. 2100-128 (8th ed. rev. 2 May 2004). Absent such a *prima facie* case, the applicant is under no obligation to produce evidence of nonobviousness. *Id.*

To establish a *prima facie* case of obviousness, three basic criteria must be met: First, there must be some suggestion or motivation, either in the references themselves or in the knowledge

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generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *Id.*

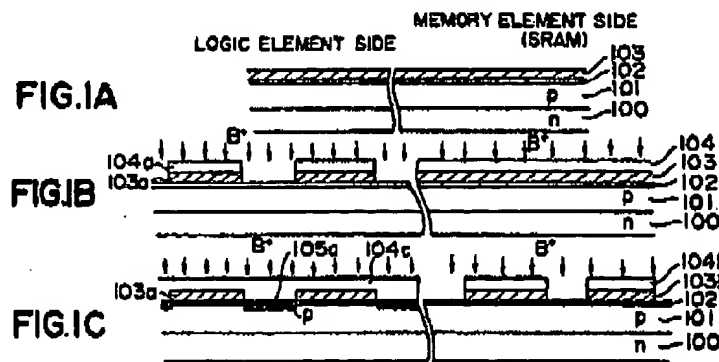
Independent claims 1 and 38 teach forming channel stop implants in a first conductivity-type region masked by an overlying patterned photoresist used to pattern an active stack to expose isolation areas in the first conductivity-type region, then forming channel stop implants in a second conductivity-type region masked by another overlying patterned photoresist used to pattern the active stack to expose isolation areas in the second conductivity-type region. The second patterned photoresist is formed directly on the exposed surface of the substrate in the isolation areas in the first conductivity-type region (i.e., no isolation oxide is grown between implants). Such a feature is not found in the cited references. *Kotah et al* teaches alternative processes for forming opposite conductivity-type wells (i.e., a p-well in an n-type substrate or a n-well in a p-type substrate), followed by channel stop implants using a single masking step, using counterdoping. No motivation exists for combining selected patterning steps from the two alternative processes as proposed in the Office Action, nor does the reference provide any reasonable expectation of success in such a selective combination.

The final Office Action states:

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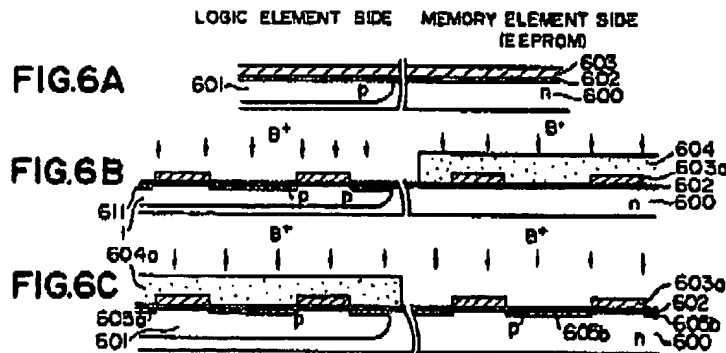
[T]he test for obviousness is not whether the features of second embodiment may be bodily incorporated into the structure of the first embodiment; nor is it that the claimed invention must be expressly suggested in any one or all of the embodiment of the invention of Katoh et al. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642, F.2d 413, 208 USPQ 871 (CCPA 1981). In this case, as mentioned above, since both embodiments of the invention described in Katoh et al. Ends up at the same stage prior to the single oxidation step (Figs. 1C and 6C), it would have been obvious to one of ordinary skill in the art at the time the invention was made to enable forming the isolation regions discloses in the second embodiment of the invention using the patterning process described in the first embodiment of the invention.

Paper No. 20050421, page 7. However *Katoh et al* teaches forming patterned photoresists separately over logic element and memory element regions – of the same conductivity type – in an integrated circuit for an SRAM:



Note that the first resist 104a remains on the nitride 103a during implantation of the channel stop dopants on the logic element side, and the second resist 104c is formed directly on the gate oxide 102 for the isolation areas in the logic element region. *Katoh et al* separately teaches use of a p-type well 601 on the logic element side of an integrated circuit for an EEPROM:

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For this process, however, the oxidation barrier is patterned before the resist layers are formed, so the first patterned layer is not formed "covering substantially all of the [n-type] region" or on the oxidation barrier remaining over active device areas in the p-type region.

The final Office Action essentially argues that the two embodiments are interchangeable, such that elements from either embodiment may be combined with or substituted for elements in the other embodiment ("[B]oth embodiments of the invention described in Katoh et al. end up at the same stage prior to the single oxidation step . . ."). This reasoning is not sufficient to establish a *prima facie* case of obviousness because it (a) fails to provide the requisite motivation or incentive for making the proposed combination or substitution (as opposed to a motivation to try the proposed combination or substitution), and (b) is not supported by the teachings of *Katoh et al.*, which is silent as to interchangeability of when the oxidation barrier is etched between the two processes. Nothing in *Katoh et al.* suggests that the extra processing steps required to form the p-type well on the logic

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element side, or the resulting structure, are conducive to use of a single patterned resist to both pattern the oxidation barrier and mask the channel stop dopant implant.

In addition, both embodiments in *Kato et al* involve implanting the same channel stop dopant (boron) in both the logic element and memory element regions, not a first channel stop dopant in the first isolation areas and a second channel stop dopant in the second isolation areas.

Therefore, the rejection of claims 1 and 32-45 under 35 U.S.C. § 103 has been overcome.

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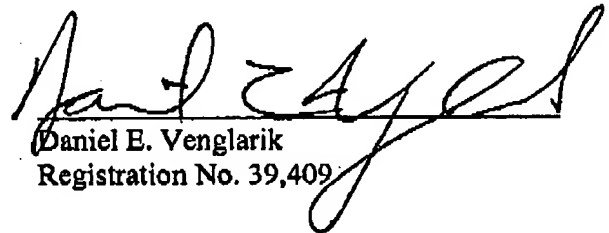
If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at *dvenglarik@davismunck.com*.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

DAVIS MUNCK, P.C.

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